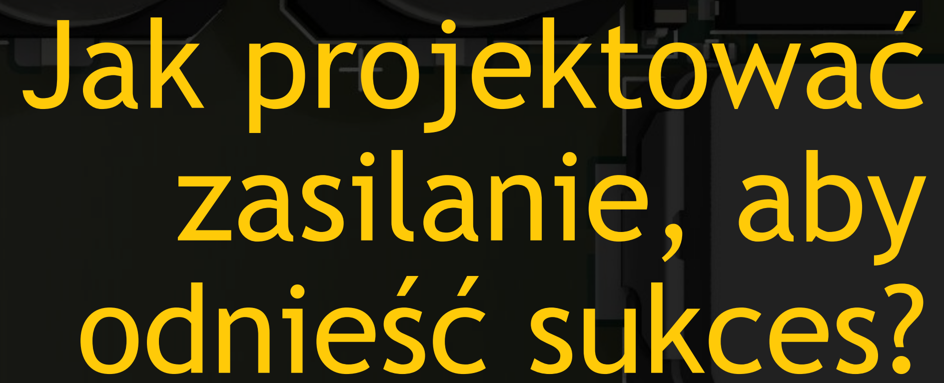
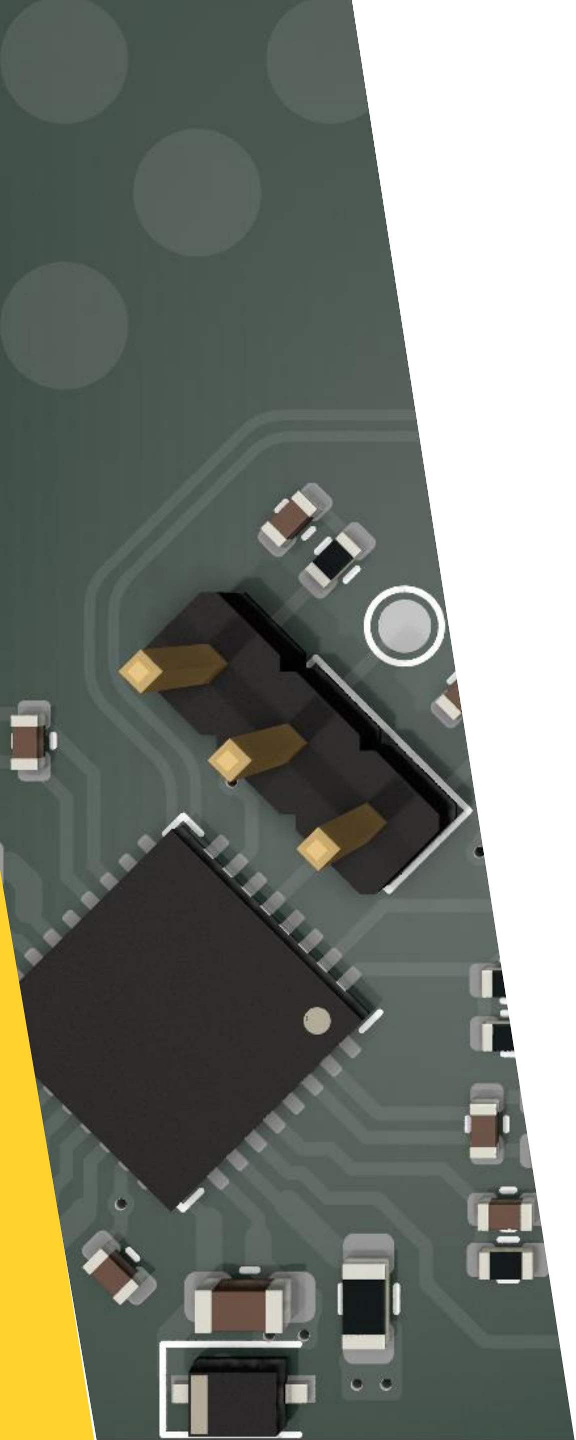


Jak projektować zasilanie, aby odnieść sukces?

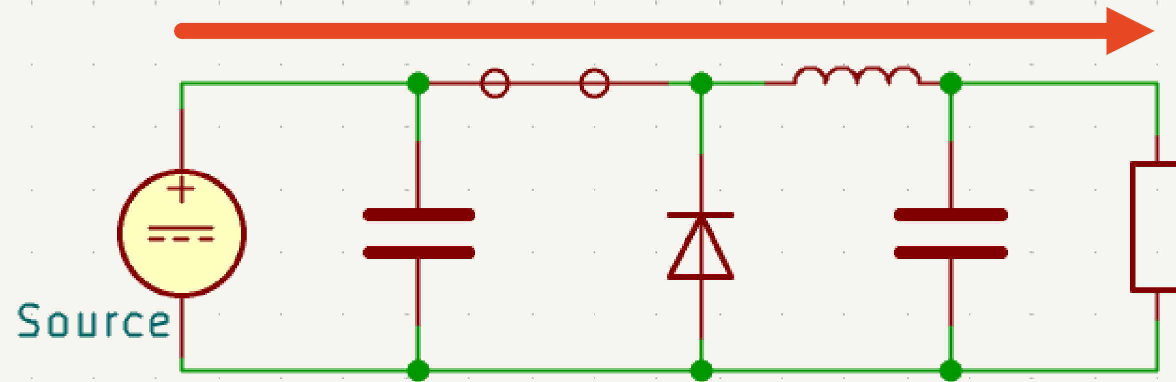
RAFAŁ KRAMEK 15.04.2024



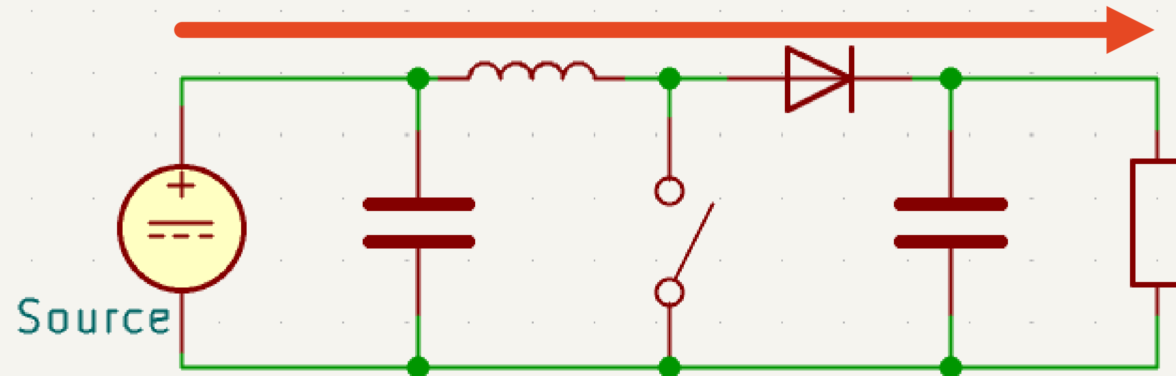
#1 Zrozum jak to działa

Topologie typu „forward” i „flyback”

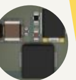
- Forward – transfer energii, kiedy klucz przewodzi



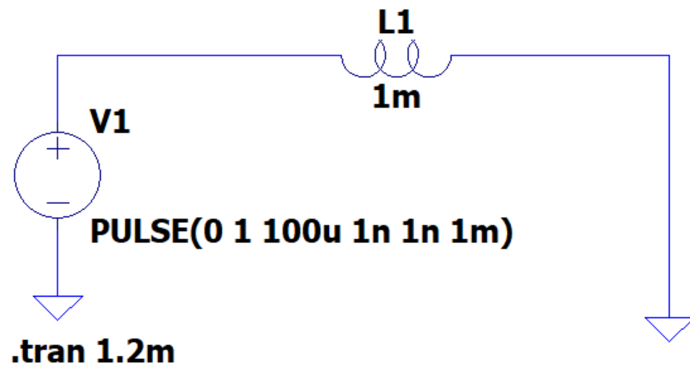
- Flyback – transfer energii, kiedy klucz nie przewodzi

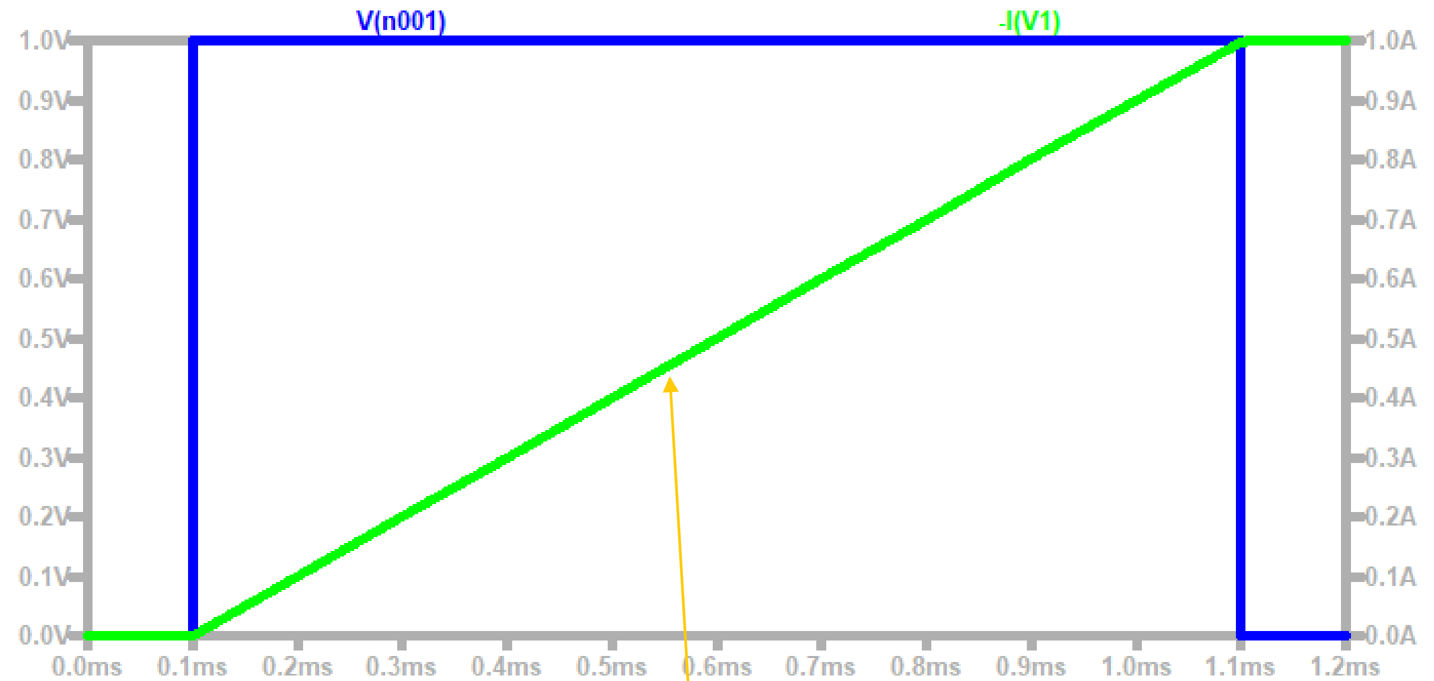


RHPZ



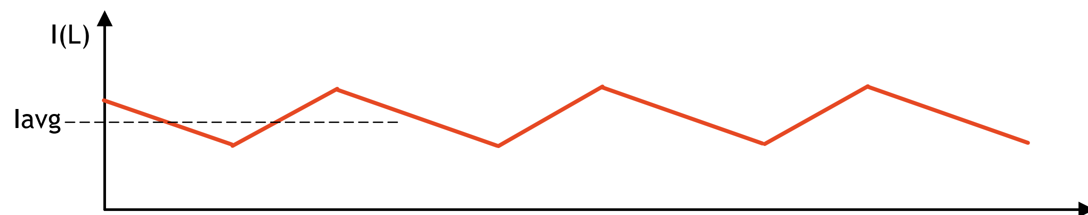
$$\frac{di}{dt}$$





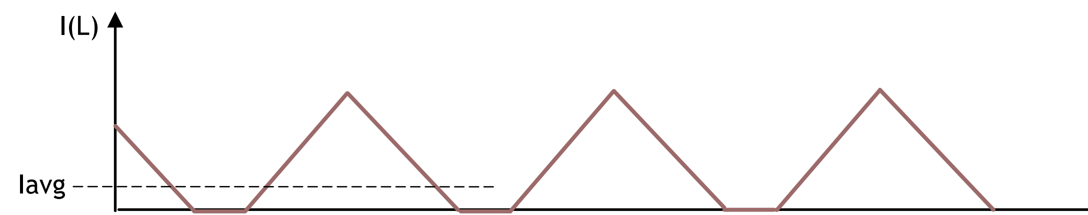
$$U = -L\frac{di}{dt} \Rightarrow \frac{U}{-L} = \frac{di}{dt} \Rightarrow m = \frac{U}{L}$$

CCM



- Większa inducyjność
- Mniejszy Iripple (EMI)
- RHPZ

DCM



- Mniejsza inducyjność
- Większy Iripple (EMI)
- RHPZ nie ma znaczenia*

File Edit Utility Help

Tektronix

Waveform View

Add New...

Cursors
Callout
Measure
Search
Results Table
Plot
More...

30 V
25 V
20 V
15 V
10
5 V
0 V
-5 V
-10 V

C 1 10 V

-2 µs
0 s
2 µs
4 µs
6 µs
8 µs
10 µs
12 µs
14 µs
16 µs

Ch 1
5 V/div
1 GHz

Ref 1
20 V/div
6.25 GS/s
Tek000_c…

Ref 2
2 V/div
6.25 GS/s
Tek000_c…

2 3 4 5 6

Add New Math
Add New Ref
Add New Bus
DVM
AFG

Horizontal
2 µs/div 20 µs
SR: 6.25 GS/s 160 ps/pt
RL: 125 kpts 7 µs

Trigger
1 10 V

Acquisition
Auto, Analyze
Sample: 8 bits
198 Acqs

Stopped
27 Nov 2023
3:22:33 AM

Buck / Step-down – „pętle” prądowe

S1

L

P3

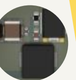
P1

P2

Cin

S2

Co



Boost / Step-up – „pętle” prądowe

L

S2

P3

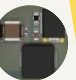
P1

P2

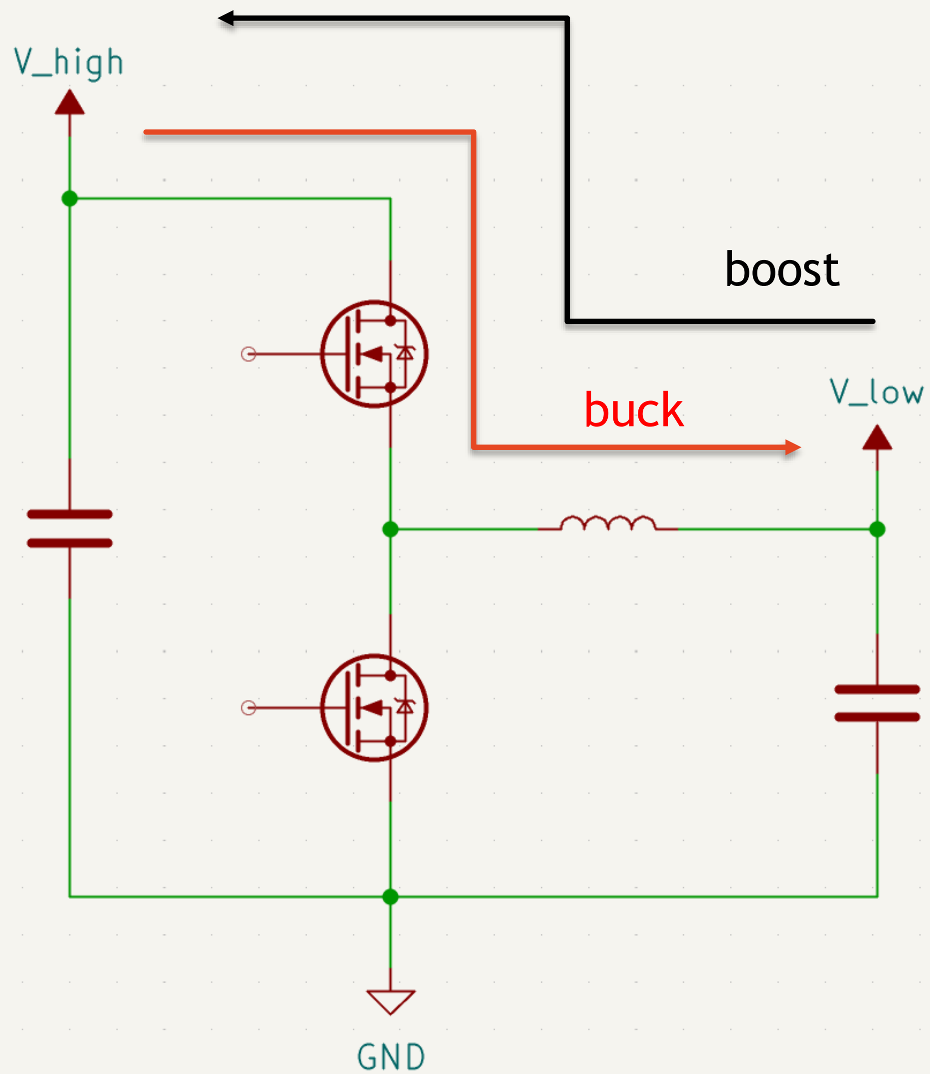
Cin

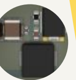
S1

Co



Buck i boost

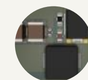




Voltage mode control

- Pojedyncza pętla kontroli
- Komparacja Vr o relatywnie wysokiej amplitudzie – duża odporność na zakłócenia
- „Trudniejsza” kompensacja

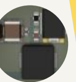
Vo
Rfb1
KOMPARATOR PWM
WZMACNIACZ BŁĘDU
Zatrzask
Q
R
S
V_REF
Rfb2
DRIVER
GND
Oscylator



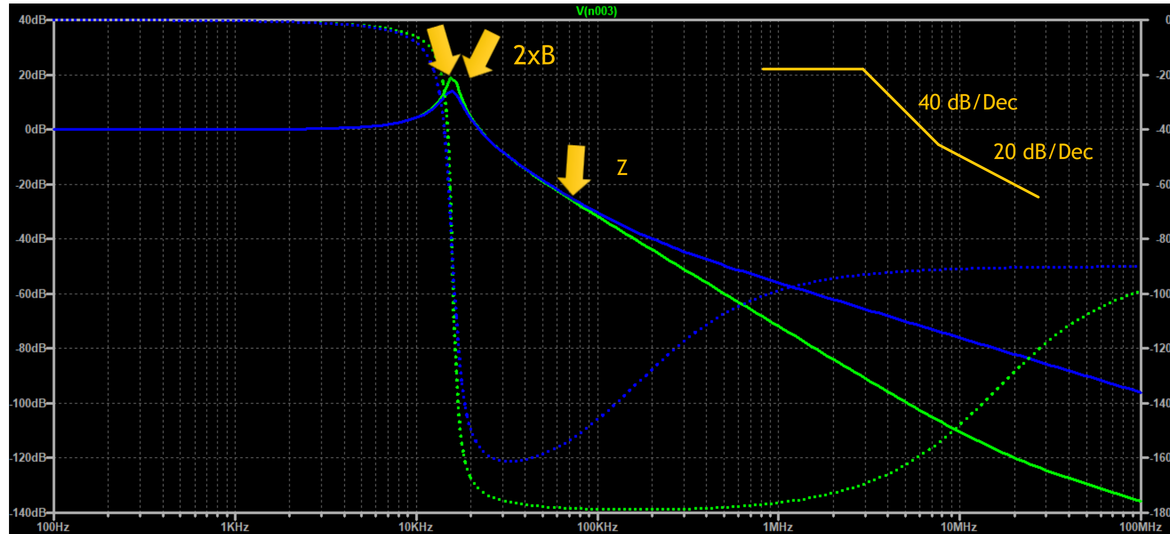
Current mode control

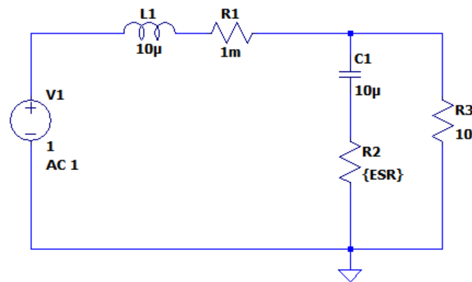
- Dwie pętlę kontroli – napięciowa i prądowa
- Komparacja Vr o niskiej amplitudzie – wrażliwa na zakłócenia
- Wbudowane ograniczenie prądowe
- „Łatwiejsza” kompensacja
- Wymaga kompensacji zbocza
- Peak current vs Average current

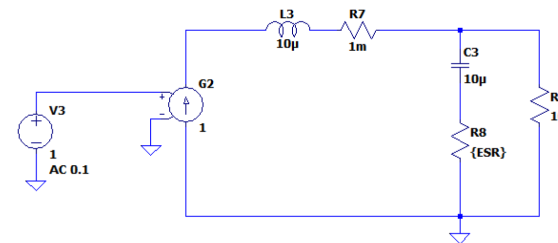
Vo
Oscylator
Rfb1
KOMPARATOR PWM
WZMACNIACZ BŁĘDU
Q
S
R
Zatrzask
DRIVER
V_REF
Rfb2
GND
Rcs
GND



Odpowiedzi filtra LC dla VMC i dla CMC







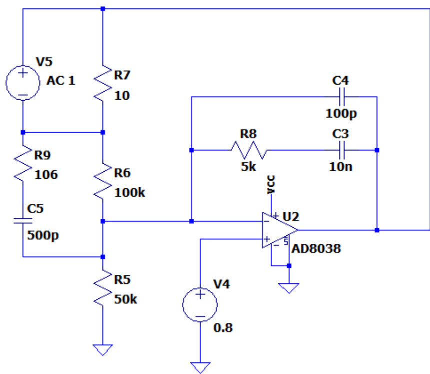
$$\omega_b = \frac{1}{\sqrt{LC}}$$

$$\omega_z = \frac{1}{ESR * C}$$

$$\omega_b = \frac{1}{C * R_{load}}$$

$$\omega_z = \frac{1}{ESR * C}$$

Kompensator typu III i typu II



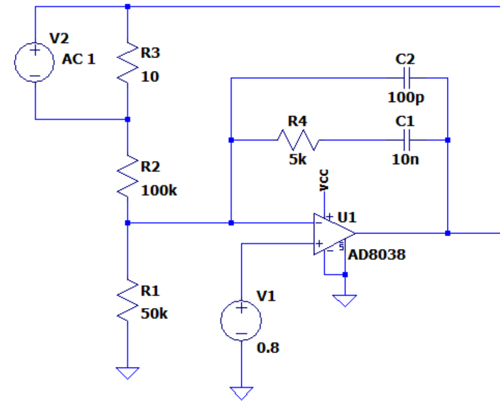
$$\omega_{b1} = \frac{1}{R_8 C_4}$$

$$\omega_{z1} = \frac{1}{R_8 C_3}$$

$$\omega_{b2} = \frac{1}{R_9 C_5}$$

$$\omega_{z2} = \frac{1}{R_6 C_5}$$

$$\omega_{z1} = \omega_{z2}$$

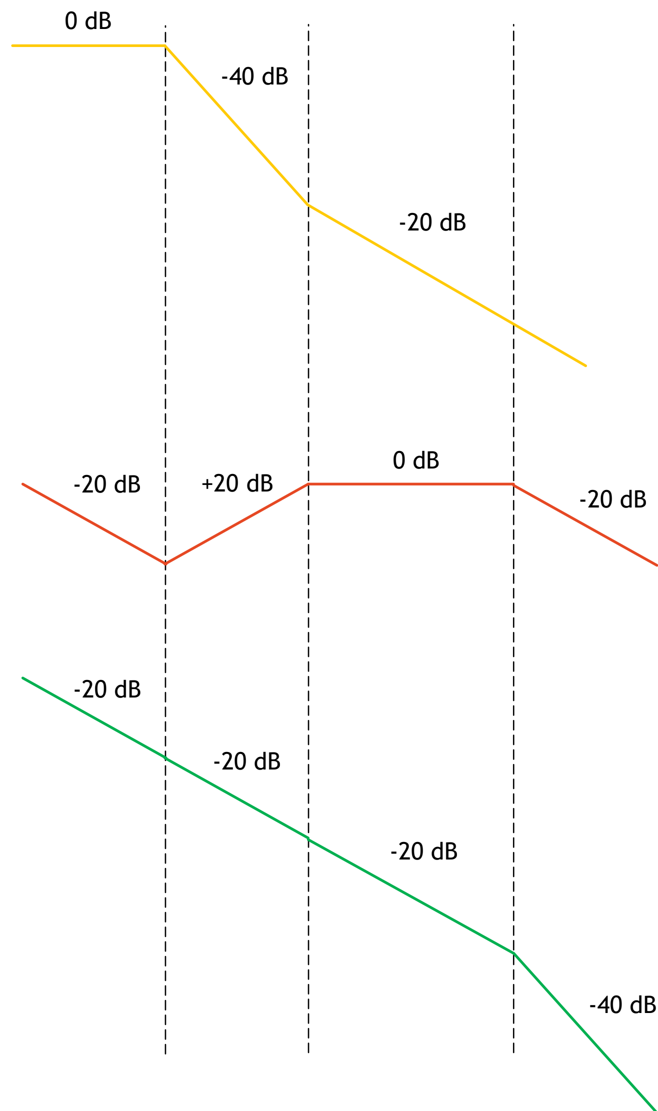


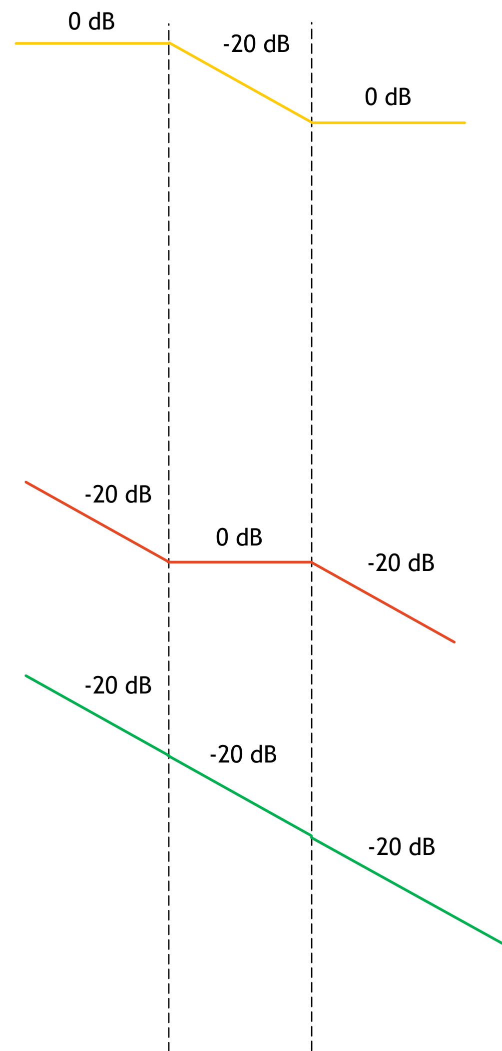
$$\omega_b = \frac{1}{R_4 C_2}$$

$$\omega_z = \frac{1}{R_4 C_1}$$

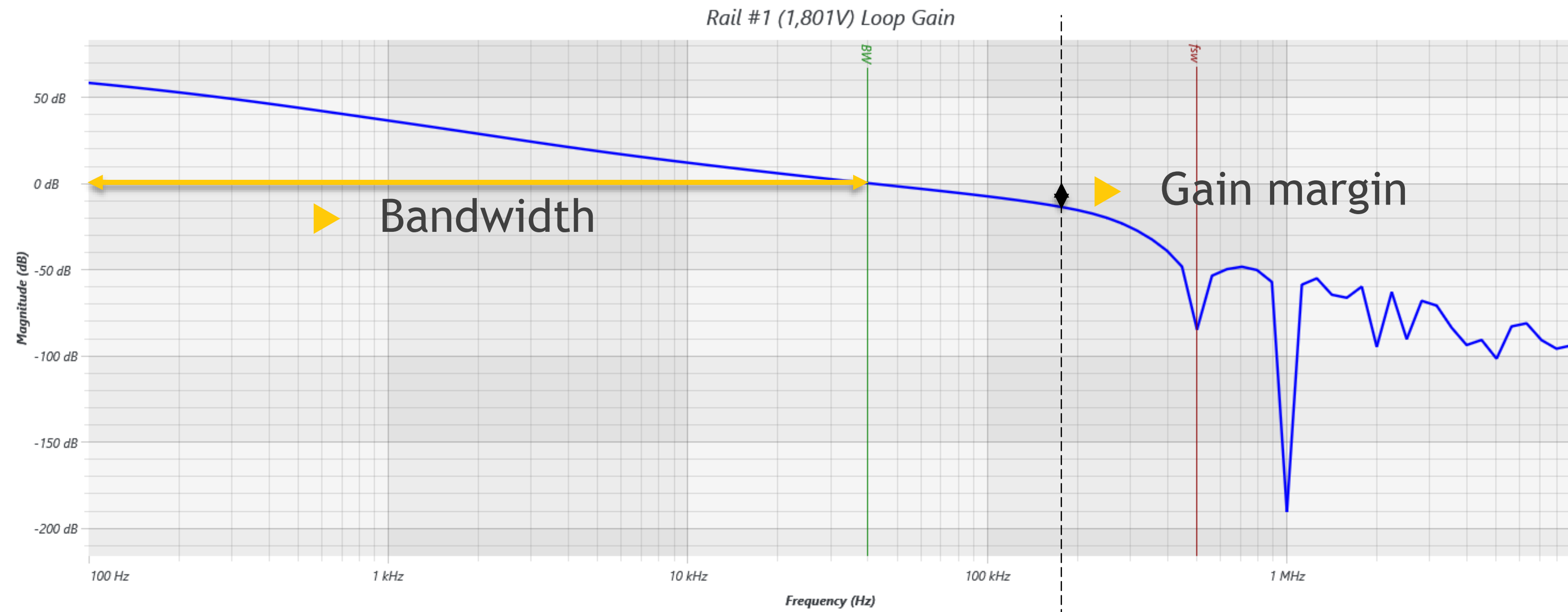
VMC CMC

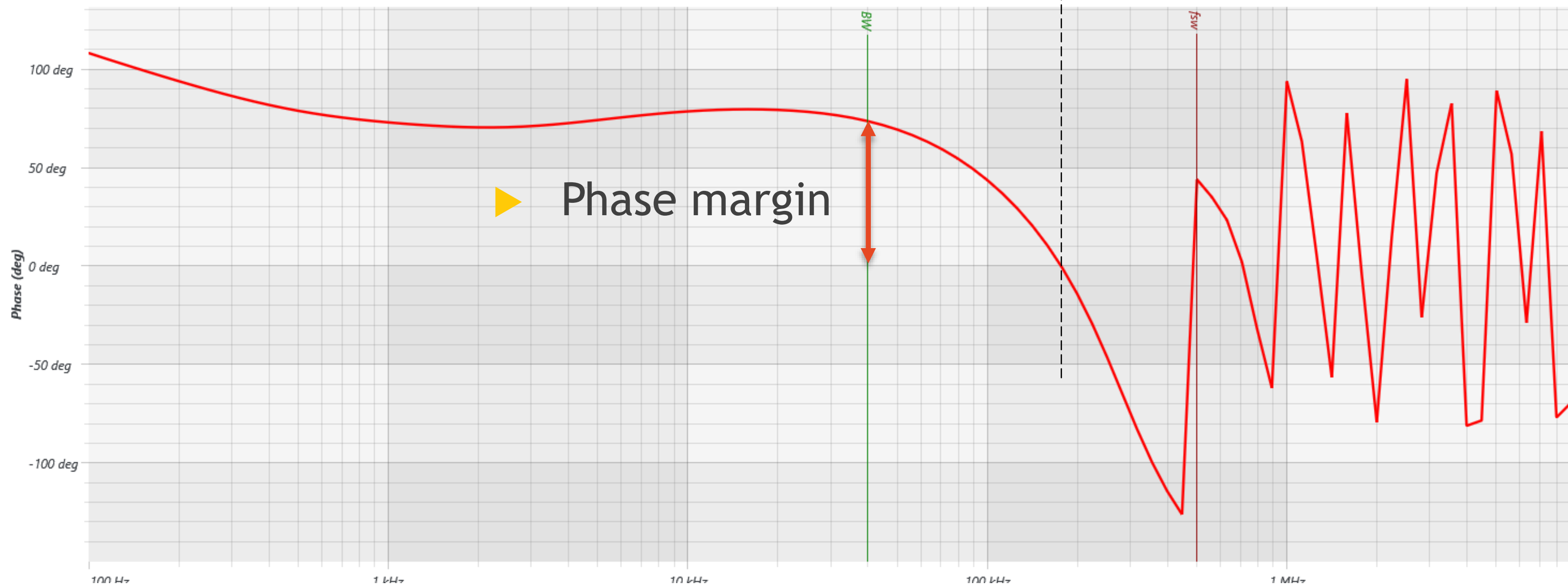
- FILTR LC
- KOMPENSATOR
- WYNIK





- Bandwidth < fs/5
- Phase margin > 45°
- Gain margin > 10 dB





About LTpowerCAD II v2.7.3

Install Ver: LTpowerCAD II v2.7.3 , Update Ver70. 2020-04-27 00:00:00

Install Date : 2023-11-28 00:00:00
Release : Customer
Last Synced : 2013-06-12 00:00:00
Username : username
Login Info Last Saved : 1111-01-01 00:00:00

For LTpowerCAD Support Contact : LTpowerCAD@analog.com

OK

#2 Bądź gotów, ale nie przesadzaj…

Just in case of EMI...

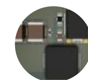
VCC
C29
100p/50V 0402
R16
1R 0603
CTR_PS_TG1
CTR_PS_TG1_R
Q2
BSC009NE2LS5
R33
1R 0603
L2
470n/38A
PH1_O
CTR_PS_SW1
TP5
TestPoint
TP8
TestPoint
C30
100p/50V 0402
D9
SS10P3CL
R17
1R 0603
CTR_PS_BG1
CTR_PS_BG1_R
Q4
BSC009NE2LS5
R34
1R 0603
GND

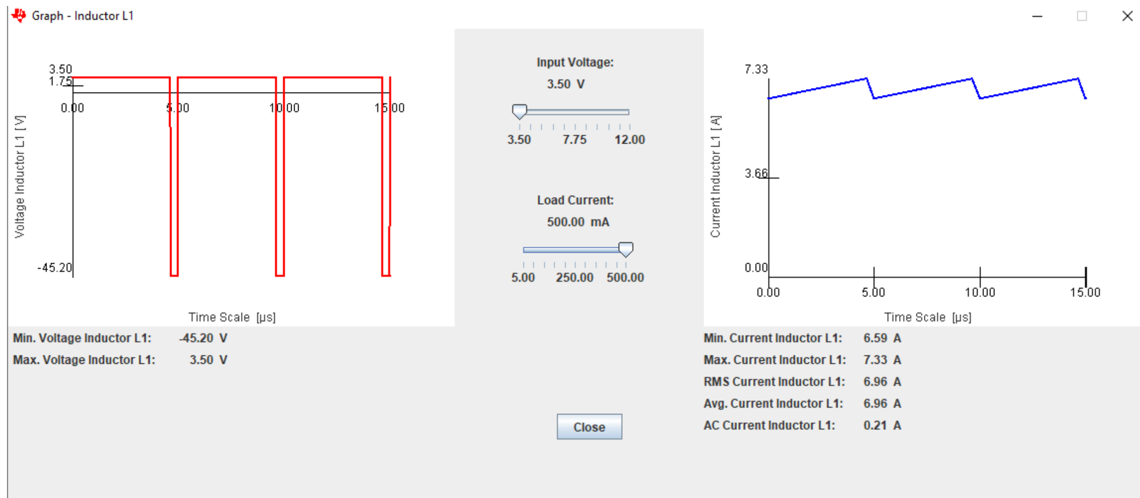
Snubber w 7 krokach

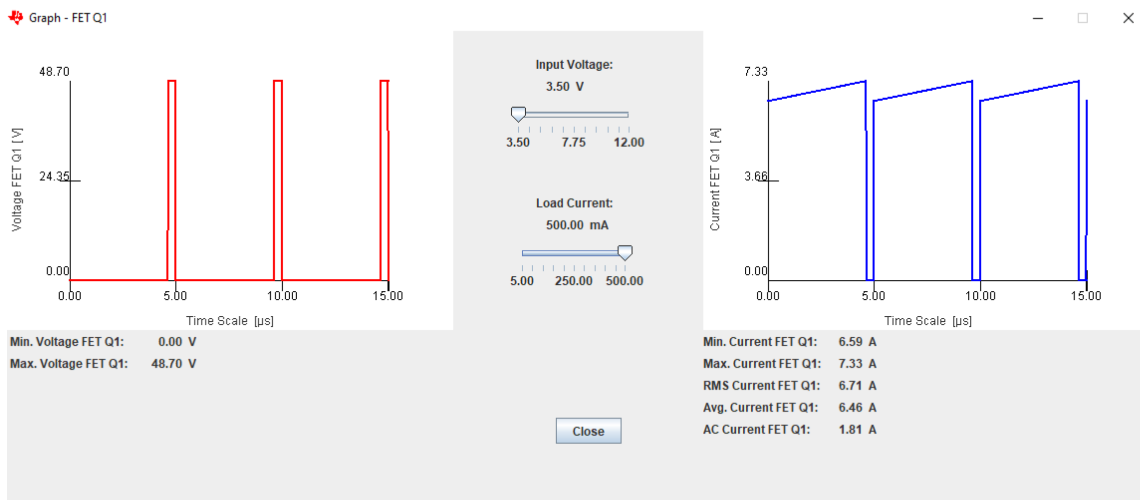
Seven steps to calculate an R-C snubber	
Step 1	Measure the circuit's oscillation frequency (f_0). See Figure 1 (top).
Step 2	Add a capacitor (C_1) in parallel with the rectifier or FET and measure the shifted oscillation frequency (f_1). Select a C_1 value that is several times larger than the rectifier's stated typical capacitance at full-reverse voltage in the data sheet. In this example, the rectifier's reverse capacitance is 22pF, so I chose a 100pF value for C_1. A frequency shift of at least 50% is reasonable. See Figure 1 (bottom).
Step 3	Calculate the frequency shift ratio: $m = \frac{f_0}{f_1}$.
Step 4	Calculate the circuit's parasitic capacitance: $C_0 = \frac{C_1}{(m^2-1)}$.
Step 5	Calculate the circuit's parasitic inductance: $L = \frac{(m^2-1)}{(2\pi f_0)^2 C_1}$.
Step 6	Calculate the starting snubber capacitor value: $C_{snub} = 3 * C_0$.
Step 7	Calculate the starting snubber-resistor value: $R_{snub} = \sqrt{\frac{L}{C_0}}$.

https://e2e.ti.com/blogs_/b/powerhouse/posts/calculate-an-r-c-snubber-in-seven-steps

#3 Nie ufaj kalkulatorom







Power Stage Designer™ Tool - Version 4.0 - Boost

File Topology Loop Calculator Tools Help

Design Values

Minimum Input Voltage:	3.5	V
Maximum Input Voltage:	12	V
Output Voltage:	48	V
Output Current:	0.5	A
Switching Frequency:	200	kHz
Diode Voltage Drop:	0.7	V
Inductor Current Ripple:	50	%

L1 D1 Ci Q1 Co

Recommended Value

Inductance: 44.57 µH

Choose Value

Inductance: 22 µH

Calculated Values at Input Voltage: 3.50 V

Period:	5.00 µs	Input Power:	24.35 W
Duty Cycle:	92.81 %	Output Power:	24.00 W
On-Time:	4.64 µs	Diode Losses:	0.35 W
Off-Time:	0.36 µs		
Zero-Time:	0.00 µs		
RHPZ:	3.59 kHz		

Load Current: 0.50 A

Input Current: 6.96 A

Current Ripple: 0.74 A 10.61 %

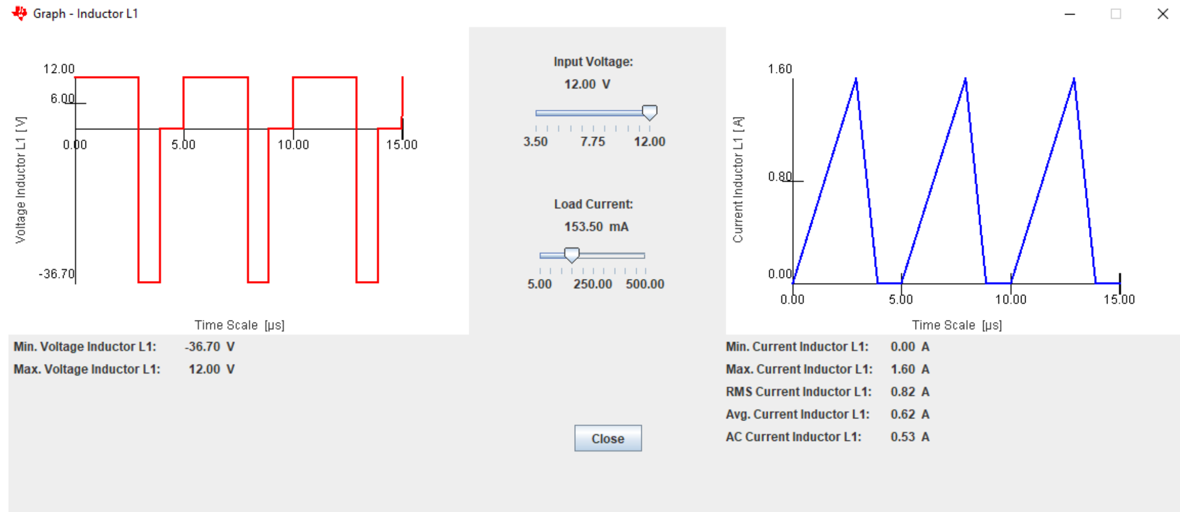
Info

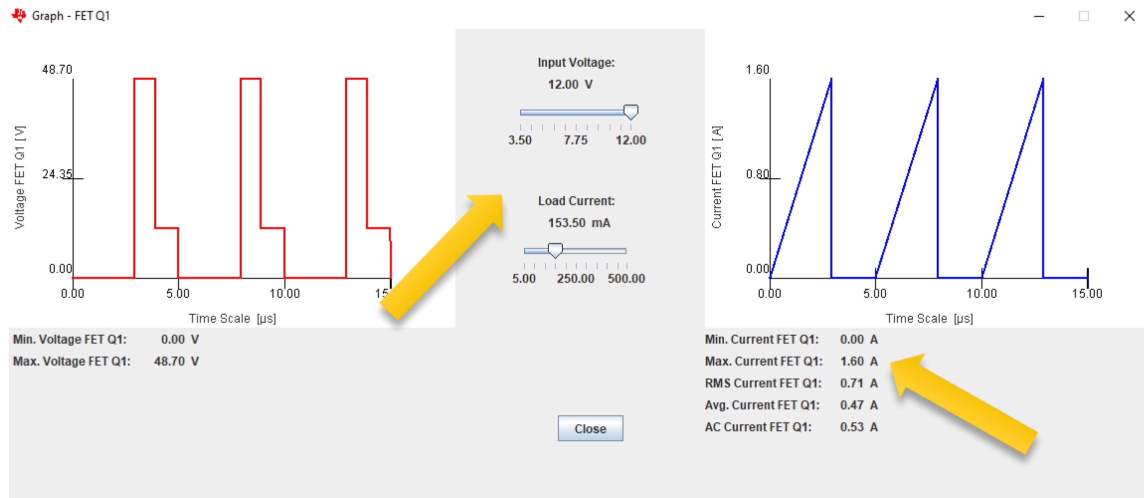
Check TIDesigns™ Reference Design Library

Start WEBENCH® Design

Texas Instruments

HDM 2024 RK





Power Stage Designer™ Tool - Version 4.0 - Boost

File Topology Loop Calculator Tools Help

Design Values

Minimum Input Voltage:	3.5	V
Maximum Input Voltage:	12	V
Output Voltage:	48	V
Output Current:	0.5	A
Switching Frequency:	200	kHz
Diode Voltage Drop:	0.7	V
Inductor Current Ripple:	50	%

L1 D1 Ci Q1 Co

Recommended Value

Inductance: 44.57 µH

Choose Value

Inductance: 22 µH

Calculated Values at Input Voltage: 12.00 V

Period:	5.00 µs	Input Power:	7.48 W
Duty Cycle:	58.67 %	Output Power:	7.37 W
On-Time:	2.93 µs	Diode Losses:	0.11 W
Off-Time:	0.96 µs		
Zero-Time:	1.11 µs		
RHPZ:	386.34 kHz		

Load Current: 0.15 A

Input Current:	0.62 A
Current Ripple:	1.60 A
	256.87 %

Info

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Texas Instruments

HDM 2024 RK

#4 Poznaj swoje tranzystory

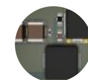


Diagram Gate charge waveforms

V_{GS}

V_{ds}

Q_g

I_d

$V_{gs(th)}$

$Q_{g(th)}$

Q_{sw}

Q_{gate}

Q_{gs}

Q_{gd}

BSC0804LS Data Sheet © Infineon

GaN vs MOSFET

Czym różni się ładowarka wykorzystująca azotek galu od tradycyjnej ładowarki z krzemu?

Ładowarki z tranzystorami wykonanymi z azotku galu znacznie różnią się od akcesoriów wykorzystujących krzem. Nowy materiał może przewodzić wyższe napięcie i dzięki niemu mniej energii tracone jest na ciepło. Oparte o GaN ładowarki są bardziej energooszczędne. Mogą dostarczyć więcej energii i ładować różne urządzenia mobilne – zarówno smartfony, jak i laptopy.

https://geex.x-kom.pl/wiadomosci/co-to-jest-ladowarka-gan/

GaN vs MOSFET

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.2 mA	100			V
I_{DSS}	Drain-Source Leakage	V_{DS} = 80 V, V_{GS} = 0 V, T_J = 25°C		0.02	0.15	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V, T_J = 25°C		0.01	1.8	mA
		V_{GS} = 5 V, T_J = 125°C		0.2	4	mA
	Gate-to-Source Reverse Leakage#	V_{GS} = -4 V, T_J = 25°C		0.01	0.18	mA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 3 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 11 A		10	13.5	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		2.0		V

Defined by design. Not subject to production test.

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	V_{DS}=V_{GS}, I_D=36 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	8.0 10.3	9.6 12.5	mΩ	V_{GS}=10 V, I_D=20 A V_{GS}=4.5 V, I_D=10 A
Gate resistance[1)]	R_G	-	1.2	1.8	Ω	-
Transconductance	g_{fs}	22	44	-	S	$\|V_{DS}\| \geq 2\|I_D\| R_{DS(on)max}$, I_D=20 A

GaN vs MOSFET

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		441	584	pF
C_{RSS}	Reverse Transfer Capacitance			3.2		
C_{OSS}	Output Capacitance			195	293	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		227		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			274		

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	1600	2100	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	250	320	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	12	21	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	4.7	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=3 Ω
Rise time	t_r	-	3.5	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=3 Ω
Turn-off delay time	$t_{d(off)}$	-	15	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=3 Ω
Fall time	t_f	-	5	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=3 Ω

GaN vs MOSFET

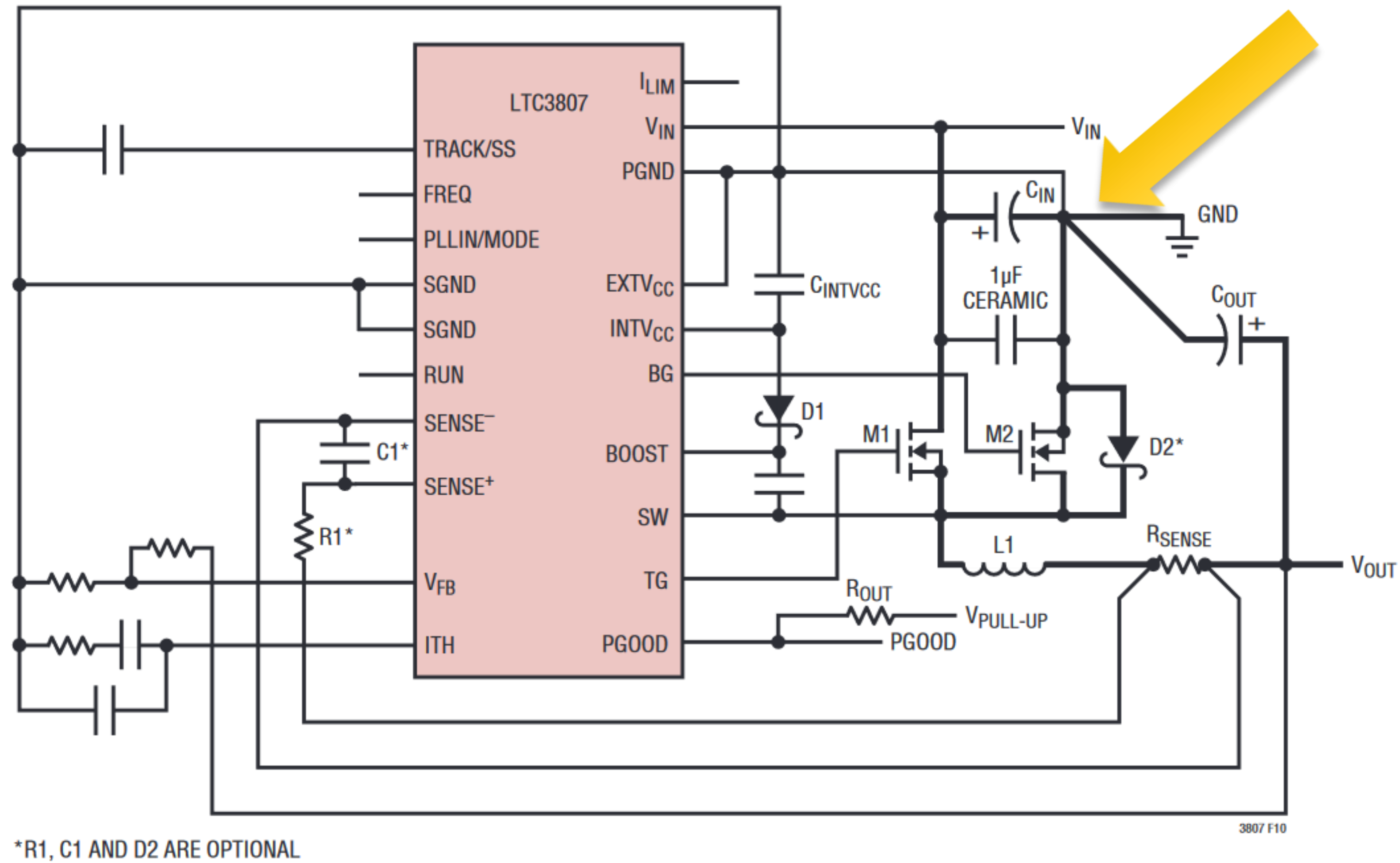
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Q_G	Total Gate Charge	$V_{DS} = 50\,V, V_{GS} = 5\,V, I_D = 11\,A$		3.5	4.5	nC
Q_{GS}	Gate to Source Charge	$V_{DS} = 50\,V, I_D = 11\,A$		1.5		
Q_{GD}	Gate to Drain Charge			0.5		
$Q_{G(TH)}$	Gate Charge at Threshold			1.0		
Q_{OSS}	Output Charge	$V_{GS} = 0\,V, V_{DS} = 50\,V$		13	20	
Q_{RR}	Source-Drain Recovery Charge			0		

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	4.6	-	nC	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	2.6	-	nC	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate to drain charge[1)]	Q_{gd}	-	4.1	6.1	nC	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	6.1	-	nC	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total[1)]	Q_g	-	12	14.6	nC	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	3.0	-	V	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	19	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1)]	Q_{oss}	-	30	40	nC	V_{DS}=50 V, V_{GS}=0 V
Reverse recovery charge[1)]	Q_{rr}	-	26	52	nC	V_R=50 V, I_F=20 A, di_F/dt=100 A/µs

#5 Optymalizuj layout tam, gdzie jest to najważniejsze

APPLICATIONS INFORMATION



*R1, C1 AND D2 ARE OPTIONAL

Figure 10. Recommended Printed Circuit Layout Diagram

LTC3807 datasheet ©ADI

V_{IN} R_{IN} C_{IN} SW D1 L1 R_{SENSE} V_{OUT} C_{OUT} R_{L1}

3807 F11

BOLD LINES INDICATE HIGH SWITCHING CURRENT. KEEP LINES TO A MINIMUM LENGTH.

Figure 11. Branch Current Waveforms

LTC3807 datasheet ©ADI

IN+

IN–

OUT+

OUT–

VDDH
BYPASS
CAPACITOR

HS GATE RETURN
PLANE (ISOLATED
FROM SWITCH
NODE)

VBST CAPACITOR

HS SOURCE
AND SINK
GATE
RESISTORS

SGND PLANE

VBST DIODE

VBST
RESISTOR

HS GaNFET

VDD
CAPACITORS

VBULK

EN RESISTOR

EN BYPASS
CAPACITOR

POWER
SWITCH
NODE

DT BYPASS
CAPACITOR

NCP51820

DT RESISTOR

LS GaNFET

VDDL BYPASS
CAPACITOR

LS SOURCE
AND SINK GATE
RESISTORS

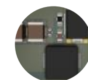
POWER PGND

LS GATE RETURN
PLANE (ISOLATED
FROM PGND)

Figure 4. NCP51820 Component Placement

NCP51820 GaN Driver, PCB Design and Layout, AND9932/D © ONSEMI

#6 Nie musi być „blisko”



10.1.3

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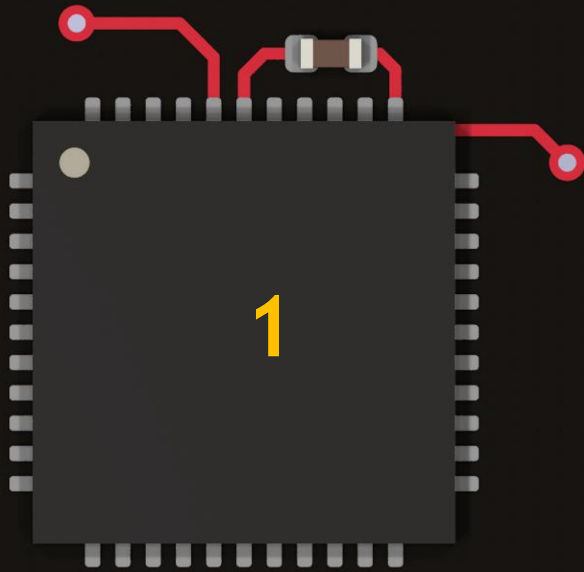
currents required by the MOSFET gate drivers.

- Minimize the lengths of the high-speed signals that run parallel to the DP and DM pair.
- Keep the DP and DM traces as short as possible.
- Route the DP and DM signals with a minimum amount of corners. Use 45-degree turns instead of 90-degree turns.
- Avoid layer changes (vias) on the DP and DM signals. Do not create stubs or branches.
- Provide the ground return vias within a 50-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- When the USB signals are not used, it is recommended that not to connect USB_OTG1_CHD_B, USB_OTG1_DN, USB_OTG1_DP, USB_OTG1_VBUS, USB_OTG2_DN, USB_OTG2_DP, USB_OTG2_VBUS pads.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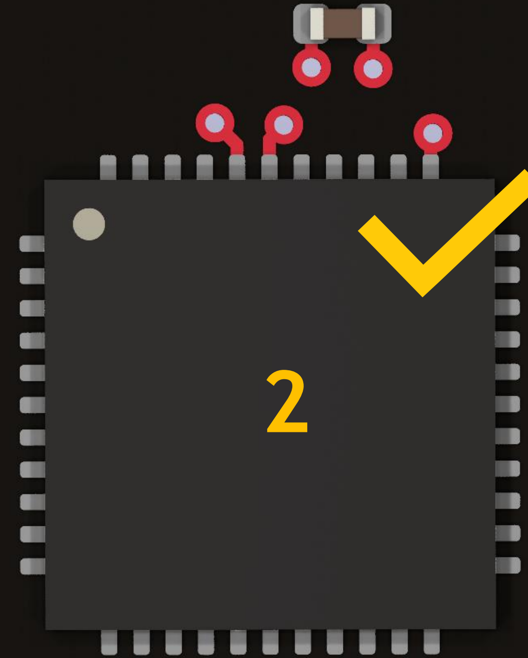
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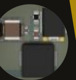
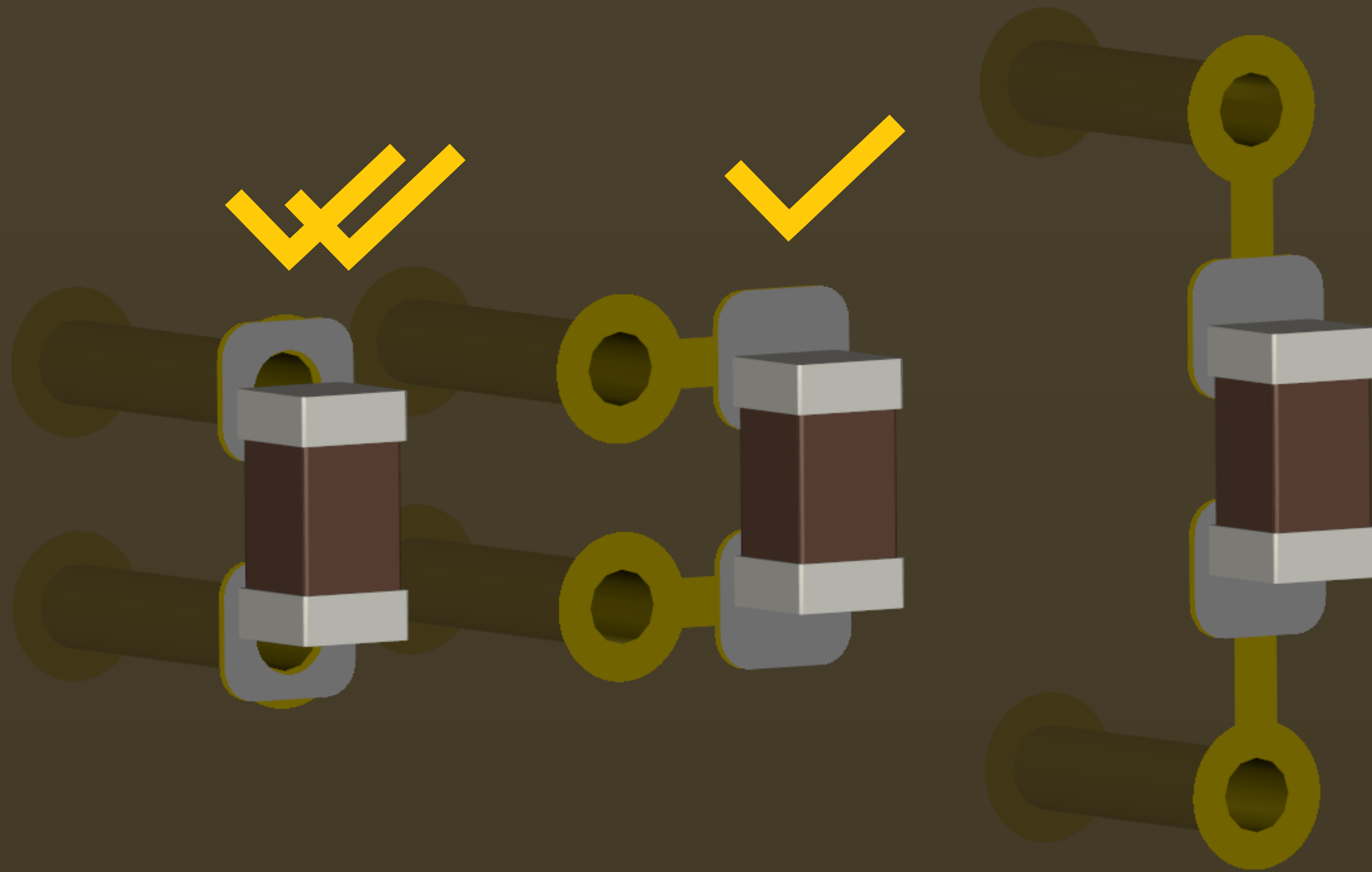
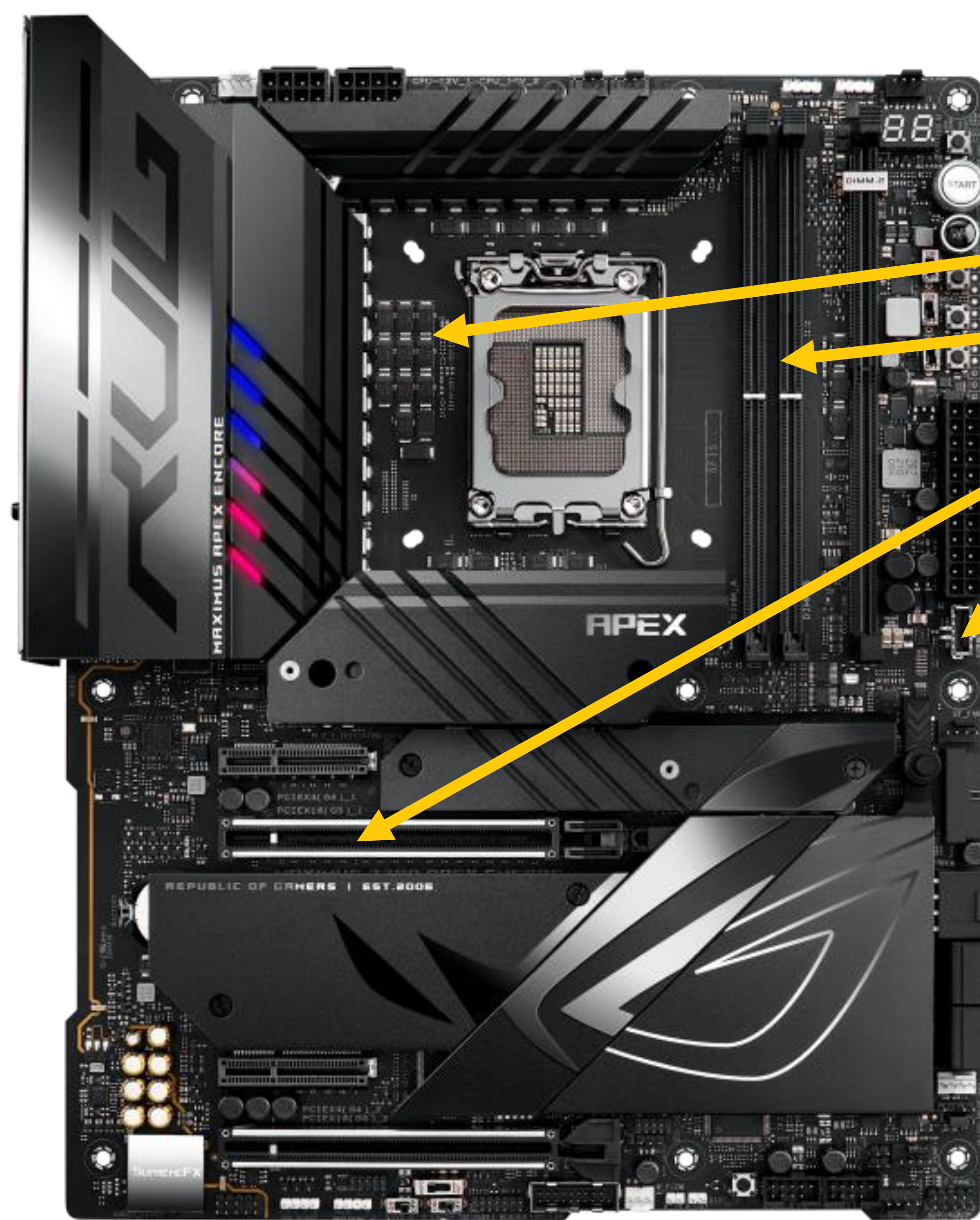




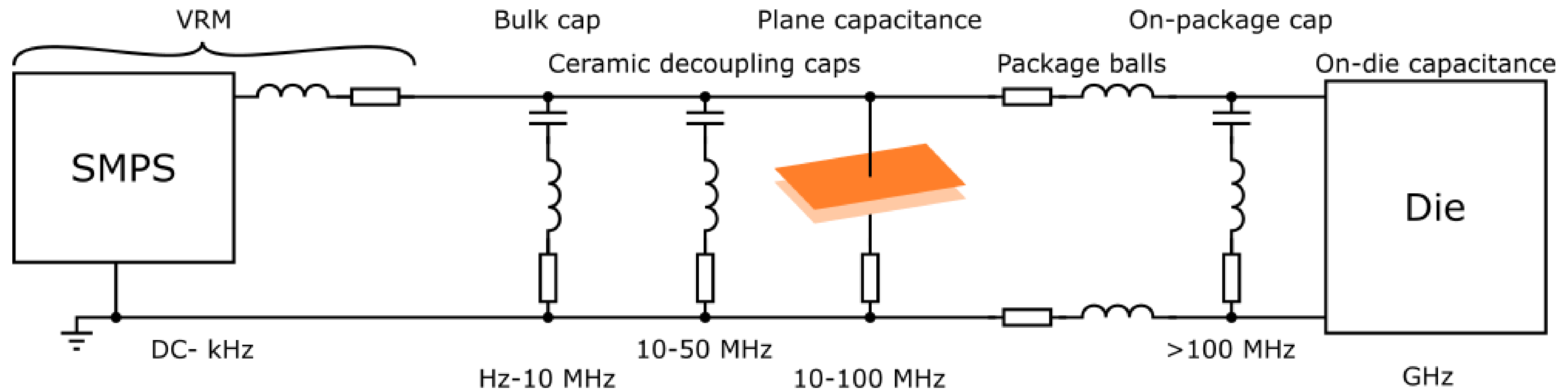


- Zasilanie ~100A
- DDR5
- PCIe 5.0
- USB 20 Gbps

https://rog.asus.com/pl/motherboards/rog-maximus/rog-maximus-z790-apex-encore/

30.5 x 24.4 cm

Co ma znaczenie w PDN?



Ztarget

V_{CCINT} operating range from the data sheet = 3%;

Assumed DC tolerance = 1%;

Therefore, allowable AC ripple = 3% – 1% = 2%.

The target impedance is calculated using the 2% AC ripple along with the current estimates from XPE for the above resource utilization to arrive at the capacitor recommendations. The equation for target impedance is:

$$Z_{target} = \frac{VoltageRailValue \times \frac{\%\ Ripple}{100}}{StepLoadCurrent} \qquad \textit{Equation 1-1}$$

V_{CCINT}, V_{CCAUX}, and V_{CCBRAM} capacitors are listed as the quantity per device, while V_{CCO} capacitors are listed as the quantity per I/O bank. Device performance at full utilization is equivalent across all devices when using these recommended networks.

https://docs.xilinx.com/v/u/en-US/ug583-ultrascale-pcb-design

Frequency Characteristic

Impedance[ohm]

100k
10k
1k
100
10
1
100m
10m
1m

100 1k 10k 100k 1M 10M 100M 1G 10G

Frequency[Hz]

In Production GRM32ER60G337ME05,|Z|,DC0V,25degC
In Production GCM32ER11A226KE11,|Z|,DC0V,25degC
In Production GRM155B31E105KA12,|Z|,DC0V,25degC
In Production GRM155R61H104KE19,|Z|,DC0V,25degC

https://ds.murata.co.jp/simsurfing/